
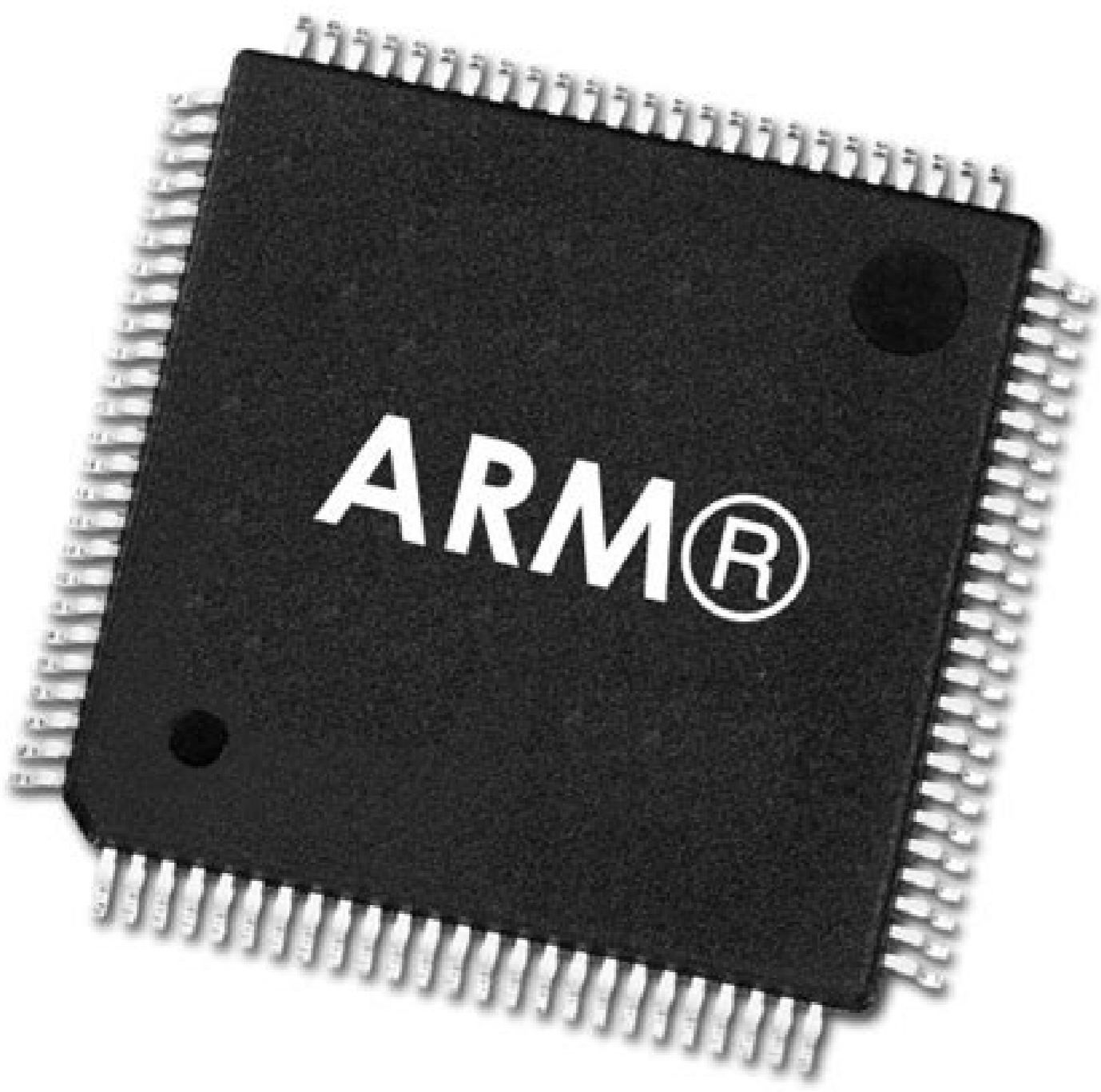


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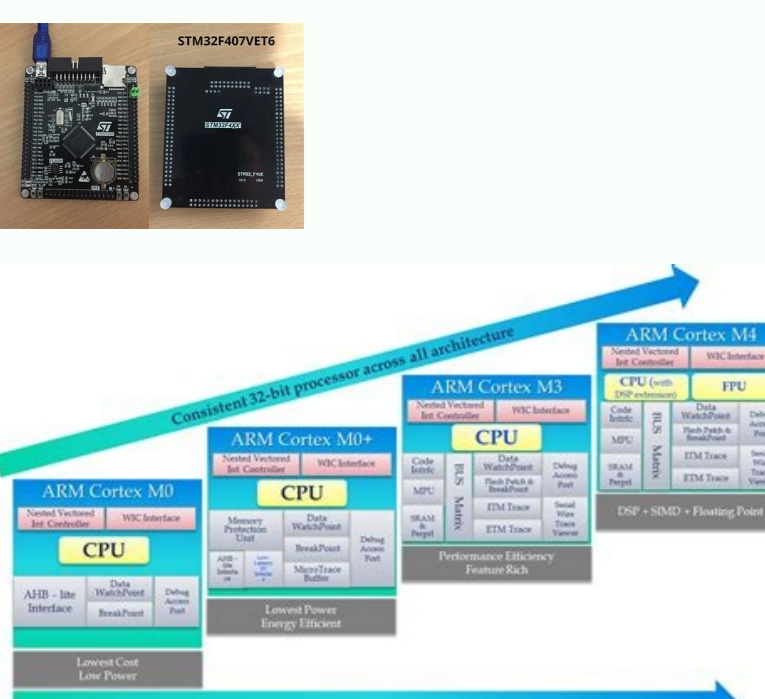
RM0041 General-purpose and alternate-function I/Os (GPIOs and AFIOs)

7.5 GPIO and AFIO register maps

Refer to Table 1: Low and medium-density device register boundary addresses and Table 2: High-density device register boundary addresses for the register boundary addresses. The following tables give the GPIO and AFIO register map and the reset values.

Table 48. GPIO register map and reset values

Offset	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	GPIOx_CRL	CNF7	MODE7	CNF6	MODE6	CNF5	MODE5	CNF4	MODE4	CNF3	MODE3	CNF2	MODE2	CNF1	MODE1	CNF0	MODE0
	Reset value	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
0x04	GPIOx_CRH	CNF15	MODE15	CNF14	MODE14	CNF13	MODE13	CNF12	MODE12	CNF11	MODE11	CNF10	MODE10	CNF9	MODE9	CNF8	MODE8
	Reset value	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
0x08	GPIOx_IDR	Reserved								IDR[15:0]							
	Reset value	0								0							
0x0C	GPIOx_ODR	Reserved								ODR[15:0]							
	Reset value	0								0							
0x10	GPIOx_BSRR	BSRR[15:0]								BSRR[15:0]							
	Reset value	0															
0x14	GPIOx_BRR	Reserved								BRR[15:0]							
	Reset value	0								0							
0x18	GPIOx_LCKR	Reserved								LCKR[15:0]							
	Reset value	0								0							



How to program arm cortex m4.

Single-cycle I/O port: Optional. 32-bit hardware integer divide (2eÅÅÅ12 cycles). Multiply instructions "64-bit result" Å ÅÅÅÅ Cortex-M3 is 3eÅÅÅ5 cycles (depending on values), Cortex-M4/M7/M33/M35P is 1 cycle. Digital Systems and Applications, Springer, Berlin, Heidelberg, Debug Access Port (DAP): None, SWD, JTAG and SWD. Note: The double-precision (DP) FPU instructions are valid in the Cortex-M7 only when the DP FPU option exists in the silicon. Cortex-M have become a popular replacements for 8-bit chips in applications that benefit from 32-bit math operations, and replacing older legacy ARM cores such as ARM7 and ARM9. TrustZone security instructions. If the Cortex-M4 / M7 / M33 / M35P has a FPU, then it is known as the Cortex-M4F / Cortex-M7F / Cortex-M33F / Cortex-M35PF.[9][10] Note: The Cortex-M series includes three new 16-bit Thumb-1 instructions for sleep mode: SEV, WFE, WFI. ^ a b c d e f g h i j k l m n o p q r ARMv7-M Architecture Reference Manual; Arm Holdings. ^ "Software repair of hard disks HDD (Google Translate)". Saturation arithmetic support. Deprecations The ARM architecture for ARM Cortex-M series removed some features from older legacy cores:[9][10] The 32-bit ARM instruction set is not included in Cortex-M cores. Unlike legacy ARM cores, the Cortex-M is permanently fixed in silicon as one of these choices. Memory Protection Unit (MPU): Provides support for protecting regions of memory through enforcing privilege and access rules. Optional Tightly-Coupled Memory (TCM): 0 to 1Å ÅMB instruction-TCM, 0 to 1Å ÅMB data-TCM, each with optional ECC. Debug probe with SWD or JTAG interface to target ARM chip, and USB or Ethernet interfaces to host computer. This allows the manufacturer to achieve custom design goals, such as higher clock speed, very low power consumption, instruction set extensions (including floating point), optimizations for size, debug support, etc. It also has a 4-stage instruction Thumb-2 (Entire). ^ a b c parai, kumar manas; Das, Banasree; Das, Gautam (January 2013). ISBNÅ. 9784883375394. The capabilities of the 32-bit arm instructions set are duplicated in many ways by the instruction sets thumb-1 and thumb-2, but some characteristics of the arm do not have a similar characteristic: the SWP and SWPB arm (SWAP) instructions do not have a similar characteristic in Cortex-M. ^ a b Renesses Official: "Cortex-M7". ^ "NEC Electronics presents 12 new 16-bit flash microcontrollers with an LCD controller / controller circuit." It has a linear address space of 16 m and 16 m byte. Note: The single-precision FPU instructions ^ n (SP) are valid on the Cortex-M4 / M7 / M33 / M35P only when there is the option ^ n SP FPU on the silicon. Definitive GuÅa of the Cortex-M0 and Cortex-M0 + processors arm; 2nd ed; Joseph Yu; 784 pages; 2015; ISBNÅ 978-0128032770. ^ Cortex-M3 DesignStart FPGA XilinxEdition ^ "Cortex-M7 Processor". In particular, the individual bits can be configured, deleted or alternated from C/C++ without performing a sequence of write modification read ^ instructions.[9][10][11] Although the bit band is optional, it is less common to find a microcontroller pon pon no om atuceje es orep .VES / IFW / EFW .IM-xetroC ed senoicurtstni sal netixie euq arap :aton .secev sod ULA ed nÅ icarepo anu azilaer .stib 61 ed oluclÅ ed senoicurtstni renetbo arap. "orud ocsid le ne BM0821 llaberIF mutnauQ :ejavlaS" .lÅ Å nis 4M-xetroC y odneitem odaste ah es M-xetroC .odasap le ne seralupop yum noreuf stib 8 ed serodalortnocrcim sol euqna Å .lanoicpo :nÅ icaruped ed nÅ icaruped al ed ollaH .M-xetroC soelcÅn sol sodot arap lanoicpÅ .RSM .SRM .BSI .BSD .BMD .LB olos .sonugla 2-bmuhT .sotad ed naidne ed odom led ahcram al ne nÅ icatummoc al etimda es on ay euqrop etixse on dneS .271 -851 .PP .Jtib46 = tib23 -Å stib 23 tib 46 ed sodatluser nec solanoicda stib 23 ed sadacilpitlum senoicurtstni eyulcni P53M / 33M / 7M / 4M / 3M-xetroC le omoc ednod ,stib 23 ojab sjÅm = tib23 Å stib 23 (stib 23 ed roirefni odatluser nu noc stib 23 ed racilpitlum senoicurtstni eneit olos 32MÅÅ / 1M / + 0M / 0M-xetroC IE :aton J0I [ 9] .RSM .SRM .BSI .BSD .BMD .LB :stib 23 ed 2-bmuhT senoicurtstni satse eyulcni olos 1M / + 0M / 0M-xetroC IE :aton J0I [ 9] .TI .ZNBC .ZBC :stib 61 ed 1-bmuhT senoicurtstni satse eyulcni on 1M / + 0M / 0M-xetroC IE :aton DBT DBT TXE dadruges .amsim al se senoicurtstni ed airanÅ nÅ icacifidoc al euqna .CVS a adardmoner euf IWS nÅ icacurtstni al .sadaseretni setrap sal a rodasecorp led arutceltuqra al ed saicnecl onis .sozÅesid solporp sus nÅ ages UPC ed sovitisopsid ednev in nacirbaf on MRA aicnecl al ed saicnetet sal .gnitexram ed savitissopaid ed etnacirbaf CI .scinortceÅ sasener [ UCM & UPM" .odavilcra ^ .Å102 ed erbutco ed 2 odarepuceÅ .j 79914 .acineÅÅ icnerer ed launam us arebil es euq atsah P53M-xetroC le arap elbinopsid [Åtse adatimil acilbÅp nÅ icarofni al :aton J1I .alrasu ratnetni ed setna nÅ icunf anu ed aicnetxse al radilav edarwot IE :aton J3I .M-xetroC ametis led oÅÅesid ed tik le odnazilltu + 0M / 0M la ragerga edeup es stib ed adnab ed nÅ icpo Å .sapate 3 ed aÅrobut [9] arutceltuqra M-6vmra Å [ nos 1M-xetroC oelcÅn led evalc sacitsÅretcarac sal .JsgnidloH UPC ed lartnec rodevevorp le omoc Åa .CI ed etnacirbaf led sotnemucod ed nÅ iceloc anu esittsnc etnemlamron MRA ed spihc sol arap nÅ icatnemucod ed eteugap nÅ in the 8-bit market, as prices of low-end Cortex-M chips have moved downward. Multiply the instructions "32 bit result" Å Å Cortex-M0 / M0 + / M23 is a silicon option ^ 1 or 32 cycle. Cortex-M1 is 3 or 33 cycle .RDA .DDA .CDA 23 2-bmuhT ÅS ÅS ÅS - ÅS ÅS on VIDU .VIDS 23 2-bmuhT ÅS ÅS ÅS ÅS ÅS ÅS RSM .SRM .BSI .BSD .BMD .LB 23 2-bmuhT ÅS ÅS ÅS ÅS ÅS ÅS on TI 6 111-bmuhT ÅS ÅS ÅS ÅS ÅS ÅS on ZBC .ZNBC 61 1-bmuhT ÅS ÅS ÅS ÅS ÅS ÅS ÅS DLEIY .IFW .EFW .HTXU .BTXU .TST .HTXS .BTXS .CVS .BUS .HRTS .BRTS .RTS .MTS .VES .CBS .BSR .ROR .HSVER .61VER .VER .HSUP .POP .RRO .NVN .LUM .VOM .RSL .LSL .HS BSRDL .HRDL .BRDL .RDL .MDL .ROE .SPC .PMC .NMC .XB .XLB .TPKB .CIB .B .RSA .DNA .RDA .DDA .CDA 61 1-bmuhT 55MxetroC P53M,33MxetroC 32MxetroC 7MxetroC 4MxetroC 3MxetroC 1M,+0M,0MxetroC senoicurtstni senoicurtstni ed opurG M-xetroC MRA senoicurtstni ed sopurG .nÅ icelus ed sozarB :1por 4M-xetroC acincÅÅ icnerer ed launam Å c b a ^ .senoiger 8 u 0 :lanoicpo JUPM( airomem ed nÅ icetorp ed dadinu :oicilis ed senoicpÅ .Å102 ed erbeitpes ed 42 .MAR ed BK Å4 .hsalf airomem ed BK Å61 noc 3M-xetroC MRA zHM ÅÅ2.CI B6T4C001F23M3TS rodalortnocrcim nu ed nereuM jorcim ygrenE( sbaL nocilS y PXN ed scl 3M-xetroC serodalortnocrcim y 0M-xetroC MRA stib 23 ed CSIR serodasecorp ed opurG .P53M/33M-xetroC MRA soelcÅn sol arap "enilniam M-6vmra" ne adicudortmep euf oicilis ed nÅ icpo al euq atsah .M-xetroC soelcÅn sol noc selbitapmoc nare on rodasecorp led senoicurtstni sal .sasener ed K87 sUCM y sUPM ed nÅ icelces ed aÅG .laiciffo sasener b Å .nÅ icelus ed sozarB :3por 33M-xetroC acincÅÅ icnerer ed launam b Å ^ .Å102 ed orerbef ed 52I noJ .sagñif Å .stib ed adnab ed nÅ iger al ne tib olos nu a airomem ed atelpmoc arbalap anu angis Å :stib ed adnab .3226 Å .lÅV .0102 SEHC .sodaregtni sametsis y ocifÅrgotpire erawdraH .)P53M/33M( 084 a 1



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