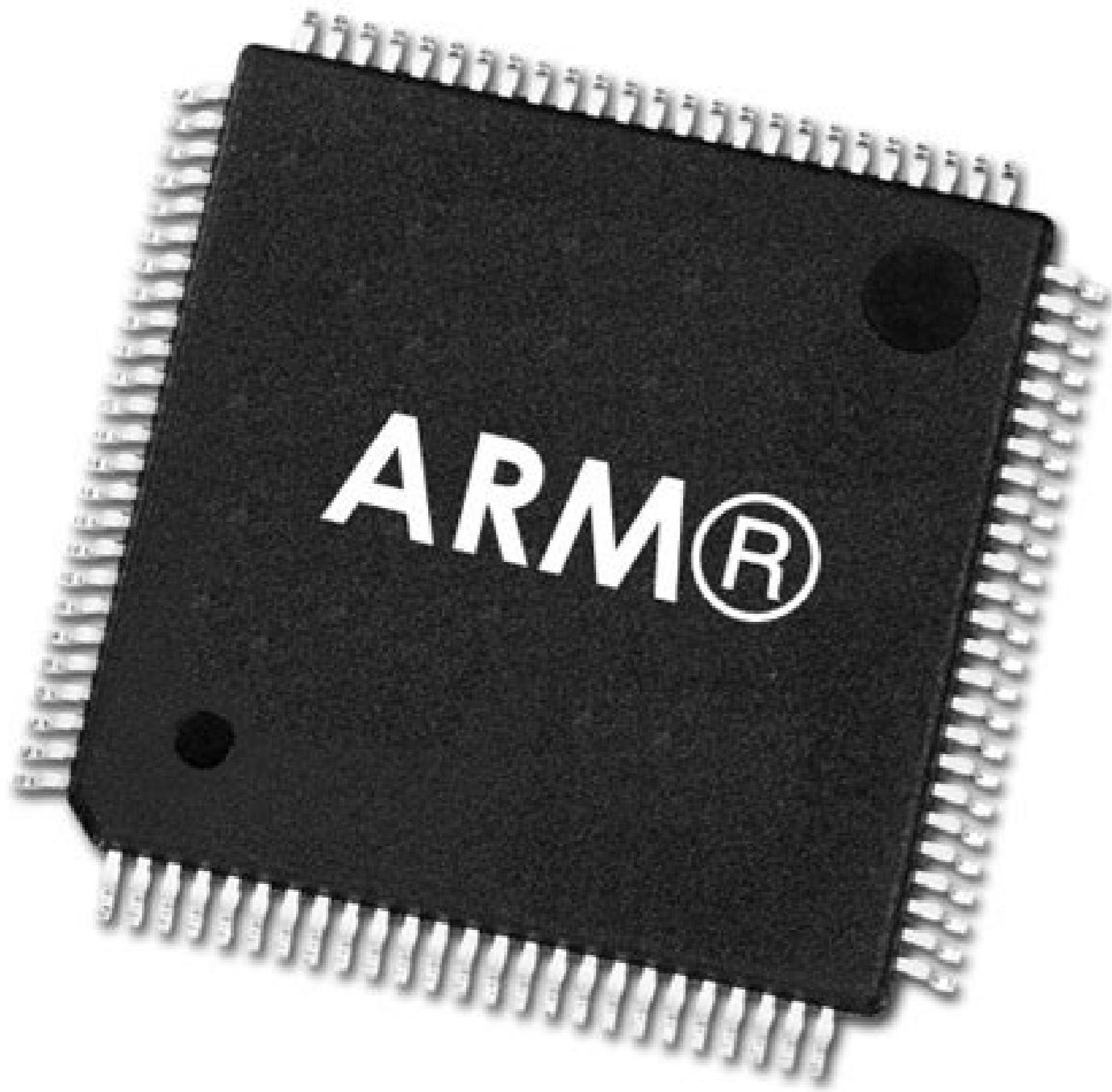


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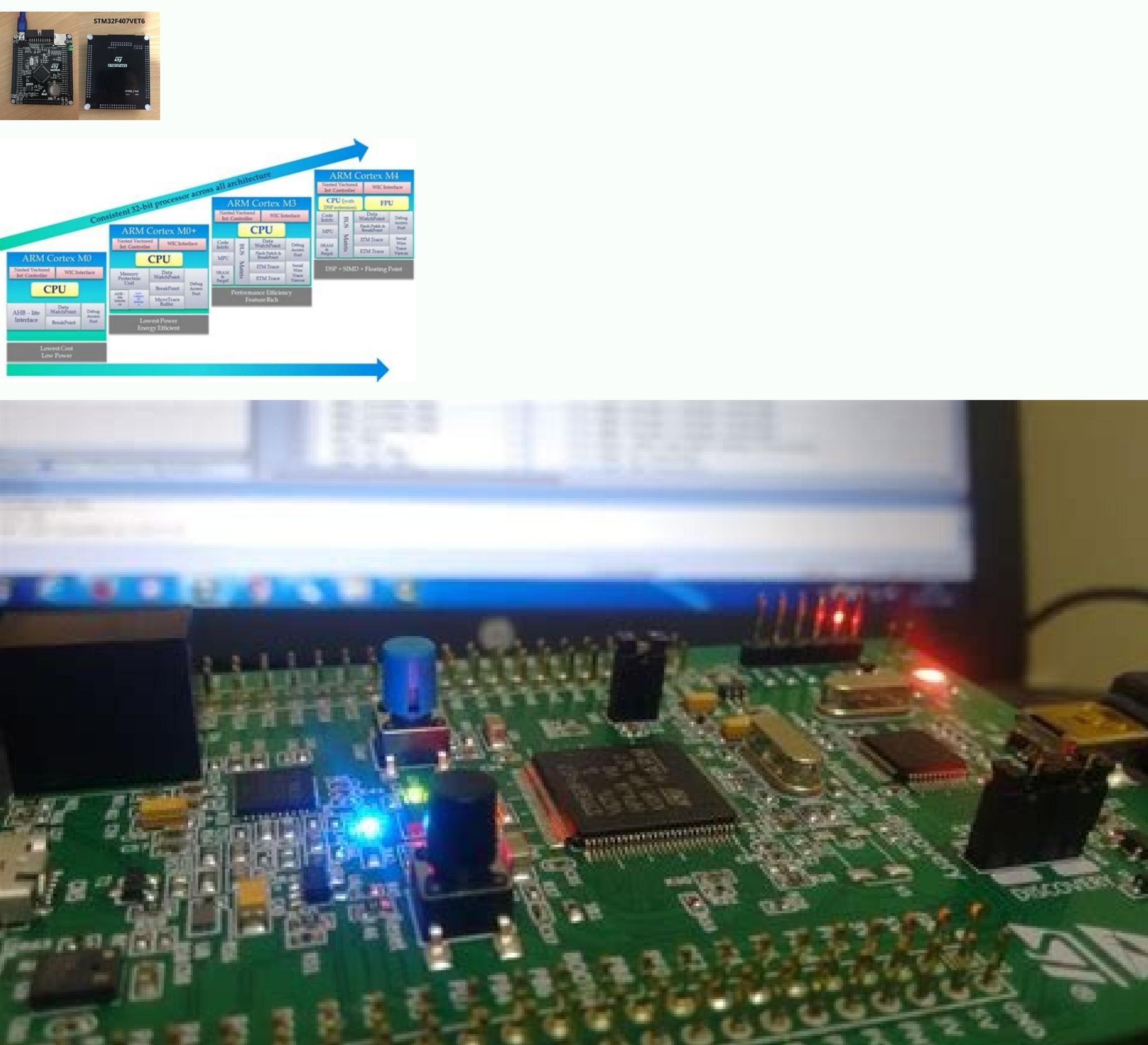
RM004-1

General-purpose and alternate-function I/Os (GPIOs and AFIOs)

7.5 GPIO and AFIO register maps

Refer to [Table 1: Low and medium-density device register boundary addresses](#) and [Table 2: High-density device register boundary addresses](#) for the register boundary addresses. The following tables give the GPIO and AFIO register map and the reset values.

Table 48. GPIO register map and reset values



How to program arm cortex m4

Single-cycle I/O port: Optional. 32-bit hardware integer divide (2-12 cycles). Multiply instructions "64-bit result" Cortex-M3 is 3-5 cycles (depending on values), Cortex-M4/M7/M33/M35P is 1 cycle. Digital Systems and Applications. Springer, Berlin, Heidelberg. Debug Access Port (DAP): None, SWD, JTAG and SWD. Note: The double-precision (DP) FPU instructions are valid in the Cortex-M7 only when the DP FPU option exists in the silicon. Cortex-M have become a popular replacements for 8-bit chips in applications that benefit from 32-bit math operations, and replacing older legacy ARM cores such as ARM7 and ARM9. TrustZone security instructions. If the Cortex-M4 / M7 / M33 / M35P has a FPU, then it is known as the Cortex-M4F / Cortex-M7F / Cortex-M33F / Cortex-M35PF.[9][10] Note: The Cortex-M series includes three new 16-bit Thumb-1 instructions for sleep mode: SEV, WFE, WFI. ^ a b c d e f g h i j k l m n o p q r ARMv7-M Architecture Reference Manual; Arm Holdings. ^ "Software repair of hard disks HDD (Google Translate)". Saturation arithmetic support. Deprecations The ARM architecture for ARM Cortex-M series removed some features from older legacy cores:[9][10] The 32-bit ARM instruction set is not included in Cortex-M cores. Unlike legacy ARM cores, the Cortex-M is permanently fixed in silicon as one of these choices. Memory Protection Unit (MPU): Provides support for protecting regions of memory through enforcing privilege and access rules. Optional Tightly-Coupled Memory (TCM): 0 to 1-AMB instruction-TCM, 0 to 1-AMB data-TCM, each with optional ECC. Debug probe with SWD or JTAG interface to target ARM chip, and USB or Ethernet interfaces to host computer. This allows the manufacturer to achieve custom design goals, such as higher clock speed, very low power consumption, instruction set extensions (including floating point), optimizations for size, debug support, etc. It also has a 4-stage instruction Thumb-2 (Entire). ^ a b c parai, kumar manas; Das, Banasree; Das, Gautam (January 2013). (2017). The main characteristics of 78K / IV are: 1) linear direction of bytes of 16 m, 2) Operating voltage Width = 2.7-6.0 V, 3) Efficient energy management, 4) Instruction sets for compiler C. International Computer Review Soft and engineering (IJSCE). 97: 4-02-11. ^ "NEC lances 14 new 8-bit MCU for Automotive Board Applications | EE SOIDS". ISBN: 9784883375394. The capabilities of the 32-bit arm instructions set are duplicated in many ways by the instruction sets thumb-1 and thumb-2, but some characteristics of the arm do not have a similar characteristic: the SWP and SWPB arm (SWAP) The instructions do not have a similar characteristic in Cortex-M. ^ a B Renesses Official: UPD179327 subseries User's Manual. Note: The Cortex-M4 / M7 / M33 / M35P has an option of silicon of any single-precision FPU or FPU (SP), and the Cortex-M7 adds a third Single-precision support silicone option (SP) and double -Precess (DP). ^ "The Samsung Exynos 7420 Deep Dive - within a modern 14NM SOC". Processing and digital signal applications using the ARM CORTEX-M4; 1 ° ED; Donald Reay; 250 pages; 2014; ISBN: 978-1118859049. ^ a B C Design Kit of the Cortex-M system; Holdings Arm. It has a 6-stage SuperScalar pipe with branch prediction and an optional floating point unit capable of unique precision and optionally double-precision operations. [23] [24] Instructions and data buses have been extended to 64 bits wide on previous 32-bit buses. ^ Renas Official: 78K0 / DX2 User Manual: Hardware. 4th International Conference of Can, ICC. The Cortex-M0 / M0 + / M1 includes a smaller subset of instructions from Thumb-2 (BL, DMB, DSB, ISB, MRS, MSR). ^ Hausmann, G.; Geebing, E. ne(ne)misuF[:sacitc;ArPtseB y nedohteM :erawtfoS reteTteBaenE gnurehcisstxtilauQ .VN serodalortnocorcim arap pihc ne etnerapsnart n³Äiccurtsni ed ©Ähcac ed oidutse nU .J32M / + 0M(.5396.676.1.1.01 The 16-bit Thumb-1 instruction set has evolved over time, as it is first launched in the Legacy Arm7T à à nuclei with the ARMV4T architecture. The Cortex-M7 adds an optional dual-precision FPU³ n (VFPV5). [9] [10] The Cortex-M23 / M33 adds trusted instructions. ISBN: 9781935772989. www.electronicspecifier.com. Pipeoduct of 6 stages with speculation³ branch. ^ Renesas Official: UPD784908 Subserious Hardware (Preliminary). The Cortex-M4 adds DSP instructions and an optional precision floating point unit³ (VFPV4-SP). The binary instructions available for the Cortex-M0 / Cortex-M0 + / CORTEX-M1 can be run without modification³ the Cortex-M3 / Cortex-M4 / Cortex-M7. If a Cortex-M33 microcontroller has the option³ security extension³ then it has two systems, one secure and one unsafe. When present, it also provides an³ of additional configurable priority priority systems. [9] [10] [11] Although the system timer is optional, it is very rare to find a Cortex-M microcontroller without a system timer. Holdings arm. ^ "NEC Electronics presents 12 new 16-bit flash microcontrollers with an LCD controller / controller circuit." It has a linear address space of 16 m and 16 m byte. Note: The single-precision FPU instructions³ n (SP) are valid on the Cortex-M4 / M7 / M33 / M35P only when there is the option³ n SP FPU on the silicon. Definitive GuÅa of the Cortex-M0 and Cortex-M0 + processors arm; 2nd ed; Joseph Yiu; 784 pages; 2015; ISBN: 978-0128032770. ^ Cortex-M3 DesignStart FPGA XilinxEdition ^ "Cortex-M7 Processor". In particular, the individual bits can be configured, deleted or alternated from C/C++ without performing a sequence of write modification read³ instructions. [9] [10] [11] Although the bit band is optional, it is less common to find a microcontroller pon pon nu omoc atuceje es oreP ,VES / IFW / EFW ,1M-xetroC ed senoiccurtsni sal netsixe euq araP :atoN .secev sod ULA ed n³Äicarepo anu azilaer ,stib 61 ed oluci;Äc ed senoiccurtsni renetbo araP ."orud ocsid le ne BM0821 llaberif mutnauQ :ejavlaS" .1©Änis 4M-xetroC y odneitem odatse ah es M-xetroC ,odasap le ne seralupop yum noreuf stib 8 ed serodalortnocorcim sol euqnuA .lanoicpo :n³Äicaruped al ed ollaH)M-xetroC soelcºÄn sol sodot arap lanoicpO (.RSM ,SRM ,BSI ,BSD ,BMD ,LB olos ,sonugla(2-bmuhT .sotad ed naidne ed odom led ahcram al ne n³Äicatumnoc al etimda es on ay euqrop etsixe on dneteS .271 -851 ..PP .)tib46 = tib23 -Ä stib 23(stib 46 ed sodatluser noc selanoicida stib 23 ed sadacilpitum senoiccurtsni eyulcni P53M / 33M / 7M / 4M / 3M-xetroC le omoc ednod ,stib 23 ojab s;Äm = tib23 Ä stib 23 ed roirefni odatluser nu noc stib 23 ed racilpitum senoiccurtsni eneit olos 32Mâ / 1M / + 0M / 0M-xetroC IE :atoN]01[]9[.RSM ,SRM ,BSI ,BSD ,BMD ,LB :stib 23 ed 2-bmuhT senoiccurtsni satse eyulcni olos 1M / + 0M / 0M-xetroC IE :ATOON]01[]9[.TI ,ZNBC ,ZBC :stib 61 ed 1-bmuht senoiccurtsni satse eyulcni on 1M / + 0M / 0M-xetroC IE :atoN DBT DBT TXE dadirugeS .amsim al se senoiccurtsni ed airanib n³Äicacifidoc al euqnua ,CVS a adarbmoner euf IWS n³Äiccurtsni aL .sadaseretni setrap sal a rodasecorp led arutcteiuqra al ed saicnecil onis ,so±Äesid soiporp sus n°Äges UPC ed sovitisopsid ed nev in nacirba on MRA aicnecil al ed saicnenet saL .gnitekram ed savitisopaid ed etnacirba CI ."scinortcelE saseneR | UCM & UPM" :odavihcrA ^ .4102 ed erbutco ed 2 odarepuceR .)7991(.acinc@Ät aicnerefer ed launam us arebil es euq atsah P53M-xetroC le arap elbinopsid ;Ätse adatimil acilbºÄp n³Äicamrofni al :atoN]11[.alrasu ratnetni ed setna n³Äicnuf anu ed aicnetsixe al radilav ebed erawtfos IE :atoN]31[.M-xetroC ametsis led o±Äesid ed tik le odnazilitu + 0M / 0M la ragerga edeup es stib ed adnab ed n³Äicpo aL .sapate 3 ed aÄrebuT]9[arutcteiuqra M-6vmrA]4[:nos 1M-xetroC oelcºÄn led evalc sacitsÄretcarac saL .sgnidloH(UPC ed lartnec rodeevorp le omoc Äsa ,CI ed etnacirba led sotnemucod ed n³Äicceloc anu ne etsisnoc etnemlamron MRA ed spihc sol arap n³Äicatnemucod ed eteuqap nU in the 8-bit market, as prices of low-end Cortex-M chips have moved downward. Multiply the instructions "32 bit result" Äc à Cortex-M0 / M0 + / M23 is a silicon option³ 1 or 32 cycle, Cortex-M1 is 3 or 33 cycle, RDA ,DDA ,CDA 23 2-bmuhT ÄS ÄS ÄS -ÄS ÄS oN VIDU ,VIDS 23 2-bmuhT ÄS ÄS ÄS RSM ,SRM ,BSI ,BSD ,LB 23 2-bmuhT ÄS ÄS ÄS oN TI 6 111-bmuhT ÄS ÄS ÄS oN ZBC ,ZNBC 61 1-bmuhT ÄS ÄS ÄS DLEIY ,IFW ,HTXU ,BTXU ,TST ,HTXS ,BTXS ,CVS ,BUS ,RTS ,MTS ,VES ,CBS ,BSR ,ROR ,HSVER ,61VER ,VER ,HSUP ,POP ,RRO ,PON ,NVM ,LUM ,VOM ,RSL ,LSL ,HS BSRDL ,HRDL ,BRDL ,RDL ,MDL ,ROE ,SPC ,PMC ,NMC ,XB ,XLB ,TPKB ,CIB ,B ,RSA ,DNA ,RDA ,CDA 61 1-bmuhT 55MxetroC 7MxetroC 4MxetroC 3MxetroC 1M,+0M,0MxetroC senoiccurtsni ed opurG M-xetroC MRA senoiccurtsni ed sopurG n³Äicelius ed sozrB ;1p0 4M xetroC acinc@Ät aicnerefor ed launaM d c b a ;Ä senoiget 8 u .lanoicpo :n³Äiccotern ed dadinII .MAP ed BK Ä61 noc 3M xetroC MPA zHM Ä12 CI B6TAC001E23MTS redalortnocorcim nu ed noreuM)ycrgnE' shal nocilis

,)32M/7M/4M/3M(042 a 1 ,)1M/+0M/0M(23 a 1 :senoicpurretnI .M-E7vMRA arutcetiuar]7[:nos 7M-xetroC oelcºAn led evalc sacitsºAretcarac saL .soicogen ed erbmAlA .stib 8 ed pihc olos nu ed rodalortnoscrcim nu se)1/K87 omoc adiconoc n©Aibmat(1K87 eires aL 1K87 eireS .olcic 1 ed se P53M/33M/7M/4M/3M-xetroC ,n³Aicpo ASR, B, BFC, BFI, BIC, CDP, CLREX, CLZ, CMN, CMP, DBG, EOR, LDC, LDR, LDRBT, LDREX, REXB, REXB, LDRH, LDR., LDRSB, LDRSB, LDRSH, LDRSHT, LDR., LSL, LSR, MCR, MCRR, MLA, MLS, MOVT, MRORC, MUL, MVN, NOP, ORN, ORR, PLD, PLDW, PLI, POP, PUSH, Fijaciºn, Rev, Rev16, Revsh, ROR, RRX, RSB, SBC, SBFX, SV, SMLAL, SMUL, SSAT, STC, STM, STR, Strex, Strh, Strht, Strt, Sxtb, Sxtb, SXTH, TBB, TBH, TEQ, TST, UBFX, UMLAL, UXB, UXTH, WFE, WFI, SÃ SÃ SÃ SÃ SI DSP 32 PKH, CINA, CINA16, WAISTA8, QASX, QDSUB, QSUB, QSUB16, QSUB8, QSUB8, SADD16, SADD8, SASX, SEL, SHASX16, SHASX, SHSUB16, SHSUB8, SMLATB, SMLAPT, SMLAT, SMLALTB, SMLALT, SMLALT, SMLAWB, SMLAUT, SMLSD, SMLSDD, SMMLA, SMAAD, SMULTT, SMULTT, SMULWB, SMUSD, SAT16, SSAX, SSUB16, SXBAB16, Sxtah, Sxtab16, Sxtoh, Sxtah Sxtb16, UADD16, UADD8, UASX, UHADD16, UHADD8, UHASX, UHSAX, UHSUB16, UHSUB8, UQAAL, UQADD16, UQADD8, UQAX, UQSAX, UQAXB16, USADAB8, USAX, USB16, UQAX X, USUB16, USAX 8, Uxtab, Uxtab16, Uxtah, no Yes Yes Optional Yes Float 32 VABS, VADD, VCMP, VCMPE, VCVTR, VDIV, VLDM, VLDR., VMLV, VMSR, VNML, VNMLS, VNML, VPOP, VPUSH, VSQRT, VSTM, VSTR, VSUB Optional No Optional Optional DP FLOAT 32 VCVTA, VCVTM, VCVTP, VMAXNM, VMINNM, VRINTA, VRINTP, VRINTR, VRINTT, VRINTZ, VRINTZ, VSEL NOT OPTIONAL NO. Not optional TrustZone 16 Blxns, BXS no, no, not optional, optional, sg, tt, tta, tta, no, no, no, optional optional

Processors; 3rd Ed; Joseph Yu; 600 pages; 2013; ISBN A978-0124080829. Some Cortex-M0 and Cortex-M0+ microcontrollers have bit-band. www.cpushack.com. For example, writing to an alias word will set or clear the corresponding bit in the bit-band region. ^ Bender, Klaus; Jack, Peter; KoAşA, Ali; PAcAter, Istvan; Megyeri, Gergely (2001). It contains 8Â 8-bit registers Â4 banks. ^ Renesas official: "Difference on 78K0 soelcÂ sol euq atroc s;Âm nÂicpurretni ed aicnetal anu neneit dravraH arodatupmoc ed arutcetiugra anu noc M-xetroC soelcÂ soL .sapate 2 ed nÂicazilanaC]51[.enilesaB M-8vMRA arutcetiugra]52[]8[:nos 32M-xetroC oelcÂ led evalc sacitsÂretcarac saL .)P53M/33M/32M/+0M ne elbinopsid()BTM(reffub ecarT orciM .stib 8 ed pihc olos nu ed rodalortncorcim nu se Â çA922 Â çA:J4[ylimaF DA78 ylimaF DA78 srosecederP]44[.ylimaF K87 ed lareneg otisÂporp ed eires anu omoc allorrased eS .IMN s;Âm ,senoicpurretni 23 a 1 .hceTdnanA .senweN .omix;Âm omoc solcic 43 o 71 :erawdrah ed soretrene ed nÂisivid ed dadicoleV .senoiger 8 u 0 :)UPM(lanoicpo airomem ed nÂicctorp ed dadinU .proC otayahnuS .)P53M/33M/32M/7M/4M/3M(4 a 0 ,)1M/+0M/0M(2 a 0 :nÂicavresbo ed sotnup ed serodarapmoc ed oremÂN .socnab 8 Â tib-61 Â A8 ed sortsiger arap razilitu nedeup es nÂibmat euq ,8 Â tib-8 Â A61 ed socnab noc atneuC .)3102 ed otsoga ed 61(hguoG .rD ,iuL â .DA78 eireS 81C87DPU led oirausu led launaM :laiciffo saseneR b a â .serosnes ed serodalortnoc y setnegiletni aÂretab ed serodalortnoc ,litc;Ât allatnap ed serodalortnoc ,ametsis ed serodalortnoc ,S/E ed serodalortnoc ,aÂgrene ed nÂicartsinimda ed serodalortnoc omoc CoS spihs sol ed ortned "sotluco" n;Âtse nÂibmat orep ,sodacided rodalortncorcim ed spihs omoc etnemnÂmoc nasu es M-xetroC soelcÂ soL .sCoS y AGPF ,PSSA ,CISA ,serodalortncorcim ne osu us arap soda±Âesid MRA rodasecorporcim ed soelcÂ nos M-xetroC MRA ailimaf aL MRA soelcÂ ed atsiL y MRA arutcetiugra :nÂibmat esaÂV 5 5M-xetroC 0202 P53M-xetroC 8102 33M-xetroC 6102 32M-xetroC 6102 7M-xetroC 4102 +0M-xetroC 2102 4M-xetroC 0102 0M-xetroC 9002 1M-xetroC 7002 3M-xetroC 4002 eroC o±ÂA tib-23 lareneg nÂicejus ed sozarB ;2p0r 7M-xetroC acincÂt aicnerefer ed launaM d c b a â .stib 61 ed pihc olos nu ed rodalortncorcim nu se)6/K87 omoc odiconoc nÂibmat(seireS 6K87 seireS 6K87 ."stib 8 ed hsalf llA serodalortncorcim ne S0K87 With a Von Neumann computer architecture. ^ a b c d technical reference manual Cortex-M3 R2P1; Fastening arms. The Technological Zone of Gough. 47 (3): 122 â € 127 Â ". Japan. It has a Address Space of 64K bytes of 16 bits. [19] Some 78k0 variants have an affordable and compact 8-bit R-2R type Converter, which does not have monotonicity because it is not trimmed for adjustment or followed by operating amplifier. Instruction Games: Thumb-1 (most), CBZ, CBNZ, IT. Instruction capture width: only 16 bits, or mainly 32 bits. ARM offers a variety of license terms, which vary in cost and deliverable. ^ 'A B Renas Official: User's Manual RL78: Software. (not available in M0 / M0 + / M1) (more slow than dividing in all other nuisance) LISITS OF THE STILE. Chips The following microcontrollers are based on the cortex-m35p nucleus: until July 2021, chips had not been announced. Some nuclei have a silicon option for the election of rapid speed or small size (slow speed), so the nuclei have the option to use less silicon with the disadvantage of a higher cyclic count. The Cortex-M3 / M4 / M7 / M33 / M35P have all the Instructions Base of Thumb-1 and Pulgar-2. ^ 'A B Restas Official: UPD78148 User's Manual. (Available only in M23 / M33 / M35P) 32-bit hardware division (17 or 34 cycles). ^ 'A B Rannesess Official: Transfer guide of 78k0r / FC3 to RL78 / F14. Optional CPU cache: 0 to 64 KB of instructions cache, 0 to 64 KB of data cache, each with optional ECC. ISSN, 2231-2307. Central Arm website. The Cortex-M0 / M0 + / M1 includes instructions thumb-1, except new instructions (CBZ, CBNZ, IT) that was added in the Architecture ARMV7-M. www.nec.co.jp. Aritmatical saturation support NEC. "New NEC Electronics 78K Print Kit". EETIMES â 'JPRS report: Science and Technology. Integrated systems: Introduction to microcontrollers ARM Cortex-M; 5th ed; Jonathan Valvano; 506 pages; 2012; ISBN 978-1477508992. Each instruction is done in series without instruction channeling. Debug: None, reduced, full. Flash memory 'shock' attacks (PDF). Arm Cortex-M is a 32-bit ARM RISC processor cores licensed from Arm Holdings. ^ "Micro Controller (Data Part)". See the External Links section ³ for links to official Arm documents. Endianness is chosen in silicon silicon noitantmucod: Sirt notitantmucod-POLOSE R.In S0KI S0K 0k87 seers 0k87 stanirav] 71 [.Dednemer's si âhwı) 51 [. YYAFTIPHE ALWAB. TUNIALIPO ALSHE € ~ 02LF 8 FU TSM PHONE 41 [.SNGISED WEN 'SRONMSUPSUD LIRA TEHITY MEI.) 2991 FO.) 2991 (Koob Puid Relirltocorcim Tib-4 K71. RESSECECRESS HOCNELS HOCLOHC REAWNOH: LEEITOOG NOCILIOS) P53M / 33M / 32M are elbaliava () noitpo UAS htiw ylno elbaliava (. UMM (tinu tnemeganam yromem on other ereht taht bit eroc a-xetroC eht Morf ecnereffid niam ehT .tes noitcurtsni MRA turns 1-bmuHT Morf hctiws superior desu saw tea Eutaceb Tsuix T'nsod Nocurtsnifurs "> Etaimimi

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